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CLAIMS

1. A method of masking data being written to a memory device, the memory device including a data bus, the method comprising:

applying masking data on the data bus;

storing the masking data in the memory device;

applying write data on the data bus;

storing the write data in the memory device; and

applying the stored masking data to mask the stored write data.

2. The method of claim 1 wherein applying masking data on the data bus and storing the masking data in the memory device occur before applying write data on the data bus and storing the write data in the memory device.

3. The method of claim 1 wherein the write data comprises a burst of data words sequentially applied on the data bus.

4. The method of claim 3 wherein all data words in the burst are stored in the memory device prior to applying the stored masking data to mask the stored data words.

5. The method of claim 3 wherein all data words in the burst are stored in the memory device prior to applying the masking data on the data bus and storing the masking data in the memory device.

6. The method of claim 3 wherein applying masking data on the data bus and storing the masking data in the memory device occur before applying the burst of write data words on the data bus.

7. The method of claim 3 wherein a portion of the data words in the burst are applied on the data bus and stored in the memory device prior to applying the masking data on the data bus and storing the masking data in the memory device, and wherein the remainder of the data words in the burst are applied on the data bus and stored in the memory device after the masking data is applied on the data bus and stored in the memory device.

8. The method of claim 3 wherein the burst comprises eight data words and the stored masking data comprises a byte of masking data, each bit in the byte being the masking data for a corresponding one of the eight data words in the burst.

9. The method of claim 1 wherein applying masking data on the data bus comprises applying a single data word on the data bus.

10. A method of transferring masking data to a memory device having a data bus, the method comprising applying masking data on the data bus and storing the masking data in the memory device.

11. The method of claim 10 wherein the masking data comprises a single word applied on the data bus.

12. The method of claim 10 wherein applying masking data on the data bus and storing the masking data in the memory device occur prior to transferring write data associated with the masking data to the memory device.

13. A method of masking data being transferred to a memory device, the memory device including a data bus, and the method comprising:

applying a sequence of data words on the data bus;

storing the sequence of data words in the memory device;

identifying at least one of the data words as being a data word containing masking data; and

applying the masking data in each identified data word to mask the data in the other data words.

14. The method of claim 13 wherein one data word in the sequence includes the masking data.

15. The method of claim 13 wherein all data words in the sequence are stored in the memory device prior to the operations of identifying at least one of the data words and applying the masking data in each identified data word.

16. The method of claim 13 wherein a portion of the data words in the sequence are applied on the data bus and stored in the memory device prior to the operations of identifying at least one of the data words and applying the masking data in each identified data word, and wherein the remainder of the data words in the sequence are applied on the data bus and stored in the memory device after the operations of identifying at least one of the data words and applying the masking data in each identified data word.

17. The method of claim 13 wherein the sequence of data words comprises nine data words, each data word being a byte and one data word corresponding to the masking data, each bit in the byte being the masking data for a corresponding one of the other eight data words.

18. The method of claim 13 wherein each data word in the sequence comprises masking data and write data.

19. A method of masking data being written to a memory device, the memory device including data, control, and address busses, and the method comprising:

applying a write partial command to the memory device over the control and address busses;

applying a sequence of data words on the data bus;

storing the sequence of data words in the memory device;

decoding the applied write partial command;

in response to the decoded write partial command,

identifying at least one of the data words as being a data word containing masking data;

applying the masking data in each identified data word to mask the data in the other data words; and

storing the masked data in addressed memory cells in the memory device.

20. The method of claim 19 wherein one data word in the sequence includes the masking data.

21. The method of claim 19 wherein all data words in the sequence are stored in the memory device prior to the operations of identifying at least one of the data words and applying the masking data in each identified data word.

22. The method of claim 19 wherein a portion of the data words in the sequence are applied on the data bus and stored in the memory device prior to the operations of identifying at least one of the data words and applying the masking data in each identified data word, and wherein the remainder of the data words in the sequence are applied on the data bus and stored in the memory device after the operations of identifying at least one of the data words and applying the masking data in each identified data word.

23. The method of claim 19 wherein the sequence of data words comprises nine data words, each data word being a byte and one data word corresponding to the masking data, each bit in the byte being the masking data for a corresponding one of the other eight data words.

24. The method of claim 19 wherein each data word in the sequence comprises masking data and write data.

25. A read/write circuit adapted to receive data words and data masking words applied on a data bus and adapted to receive read data from a memory-cell array, the read/write circuit operable during a read mode to apply read data received from the array on the data bus, and operable during a write-partial mode to store at least one data masking word and at least one data word applied on the data bus, and operable to apply each data masking word to mask each data word and to thereafter apply each masked data word to the memory-cell array.

26. The read/write circuit of claim 25 wherein the data masking word includes masking data for masking and not masking corresponding segments of data contained in the data words.

27. The read/write circuit of claim 26 wherein each segment comprises a byte of data.

28. The read/write circuit of claim 25 wherein the read/write circuit receives all data masking words prior to receiving the data words.

29. The read/write circuit of claim 25 wherein the read/write circuit is further operable during a write mode to receive and store data words over the data bus and apply the data words to the memory-cell array.

30. The read/write circuit of claim 25 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

31. The read/write circuit of claim 30 wherein all data words in the burst are stored in read/write circuit prior to the read/write circuit applying the data masking word to mask the data words.

32. The read/write circuit of claim 30 wherein the read/write circuit stores a portion of the data words in the burst prior to storing the data masking word, and wherein the read/write circuit stores the remainder of the data words in the burst after storing the data masking word.

33. The read/write circuit of claim 25 wherein the received at least one data masking word and data word comprise a single word including masking data and write data to be masked.

34. A read/write circuit adapted to receive data words and data masking words applied on a data bus and adapted to receive read data from a memory-cell array, the read/write circuit operable during a read mode to apply read data received from the array on the data bus, and operable during a write mode to store data words applied on the data bus and apply the data words to the memory-cell array, and operable during a write-partial mode to store at least one data masking word and at least one data word applied on the data bus, and operable to apply masking data contained in each data masking word to selectively

mask and not mask data contained in each data word, and to thereafter apply the masked and not masked data to the memory-cell array.

35. The read/write circuit of claim 34 wherein the data masking word includes masking data for masking and not masking corresponding segments of data contained in the data words.

36. The read/write circuit of claim 35 wherein each segment comprises a byte of data.

37. The read/write circuit of claim 34 wherein the read/write circuit receives all data masking words prior to receiving the data words.

38. The read/write circuit of claim 34 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

39. The read/write circuit of claim 38 wherein during the write-partial mode of operation all data words in the burst are stored in read/write circuit prior to the read/write circuit applying the data masking word to mask the data words.

40. The read/write circuit of claim 38 wherein the read/write circuit stores a portion of the data words in the burst prior to storing the data masking word, and wherein the read/write circuit stores the remainder of the data words in the burst after storing the data masking word.

41. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder and control circuit;

a read/write circuit coupled to the data bus and the memory-cell array, the read/write circuit operable during a read mode to apply read data received from the memory-cell array on the data bus, and operable during a write-partial mode to receive at least one data masking word and at least one data word applied on the data bus and store the received words, and operable to apply each data masking word to mask each data word and to thereafter apply each masked data word to the memory-cell array.

42. The memory device of claim 41 wherein the memory comprises a double-data rate synchronous dynamic random access memory.

43. The memory device of claim 41 wherein the read/write circuit receives all data masking words prior to receiving the data words.

44. The memory device of claim 41 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

45. The memory device of claim 44 wherein all data words in the burst are stored in the read/write circuit prior to the read/write circuit applying the data masking word to mask the data words.

46. The memory device of claim 44 wherein the read/write circuit stores a portion of the data words in the burst prior to storing the data masking word, and wherein the read/write circuit stores the remainder of the data words in the burst after storing the data masking word.

47. The memory device of claim 44 wherein the received at least one data masking word and data word comprise a single word including masking data and write data to be masked.

48. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder and control circuit;

a read/write circuit coupled to the data bus and the memory-cell array, the read/write circuit operable during a read mode to apply read data received

from the memory-cell array on the data bus, and operable during a write-partial mode to receive at least one data masking word and at least one data word applied on the data bus and store the received words, and operable to apply each data masking word to mask each data word and to thereafter apply each masked data word to the memory-cell array.

49. The computer system of claim 48 wherein the memory comprises a double-data rate synchronous dynamic random access memory.

50. The computer system of claim 48 wherein the read/write circuit receives all data masking words prior to receiving the data words.

51. The computer system of claim 48 wherein the data words comprise a burst of data words sequentially applied on the data bus and the data masking word comprises a single data masking word.

52. The computer system of claim 51 wherein all data words in the burst are stored in the read/write circuit prior to the read/write circuit applying the data masking word to mask the data words.

53. The computer system of claim 51 wherein the read/write circuit stores a portion of the data words in the burst prior to storing the data masking word, and wherein the read/write circuit stores the remainder of the data words in the burst after storing the data masking word.

54. The computer system of claim 51 wherein the received at least one data masking word and data word comprise a single word including masking data and write data to be masked.